- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Active-High and Active-Low Enables**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates From Single 5-V Supply**
- **Logically Interchangeable With AM26LS31**

N PACKAGE
(TOP VIEW)

1A	1	16	V_{CC}
1Y	2	15	4A
1Z	3	14	4Y
G	4	13	4Z
2Z	5	12	$\overline{G}$
2Y	6	11	3Z
2A	7	10	3Y
GND	8	9	3A

DW PACKAGE
(TOP VIEW)

1A	1	20	V_{CC}
1Y	2	19	4A
NC	3	18	4Y
1Z	4	17	NC
G	5	16	4Z
2Z	6	15	$\overline{G}$
NC	7	14	3Z
2Y	8	13	NC
2A	9	12	3Y
GND	10	11	3A

NC – No internal connection

description

The SN75172 is a monolithic quadruple differential line driver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges, making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75172 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS
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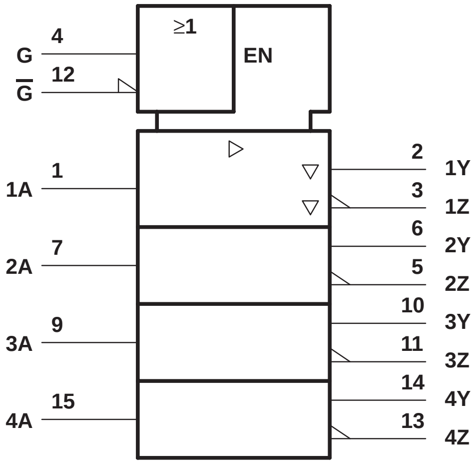
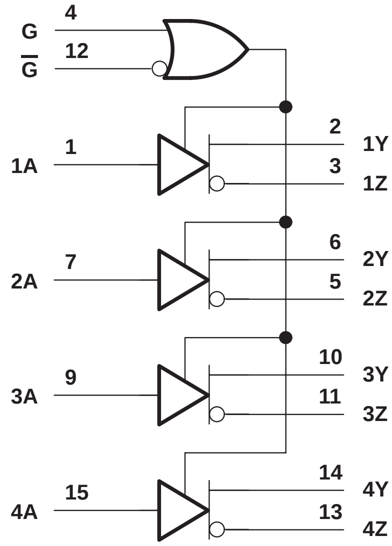
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers shown are for the N package.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Voltage range at any bus terminal . . . . –10 V to 15 V
Input voltage, V_I . . . . 5.5 V
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			–7 to 12	V
High-level output current, I_{OH}			–60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA			–1.5	V
V_O	Output voltage	I_O = 0	0		6	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –33 mA		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = 33 mA		1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0	1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1	1/2 V_{OD1} or 2‡			V
		R_L = 54 Ω, See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω, See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage¶				+3 – 1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§				±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = – 7 V to 12 V			±100	µA
I_{OZ}	High-impedance-state output current	V_O = – 7 V to 12 V			±100	µA
I_{IH}	High-level input current	V_I = 2.7 V			20	µA
I_{IL}	Low-level input current	V_I = 0.5 V			–360	µA
I_{OS}	Short-circuit output current	V_O = – 7 V			–180	mA
		V_O = V_{CC}			180	
		V_O = 12 V			500	
I_{CC}	Supply current (all drivers)	No load, Outputs enabled		38	60	mA
		No load, Outputs disabled		18	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 2: See Figure 3-5 of EIA Standard RS-485.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1}\rvert$	V_o	V_o
$\lvert V_{OD2}\rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD2}\rvert$		V_t (Test Termination Measurement 2)
$\Delta\lvert V_{OD}\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$
V_{OC}	$\lvert V_{os}\rvert$	$\lvert V_{os}\rvert$
$\Delta\lvert V_{OC}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$
I_{OS}	$\lvert I_{sa}\rvert, \lvert I_{sb}\rvert$	
I_O	$\lvert I_{xa}\rvert, \lvert I_{xb}\rvert$	I_{ia}, I_{ib}

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω, See Figure 2		45	65	ns
$t_{t(OD)}$	Differential-output transition time			80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 4		45	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 3		78	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 4		18	30	ns

PARAMETER MEASUREMENT INFORMATION

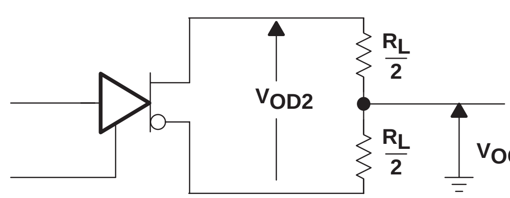
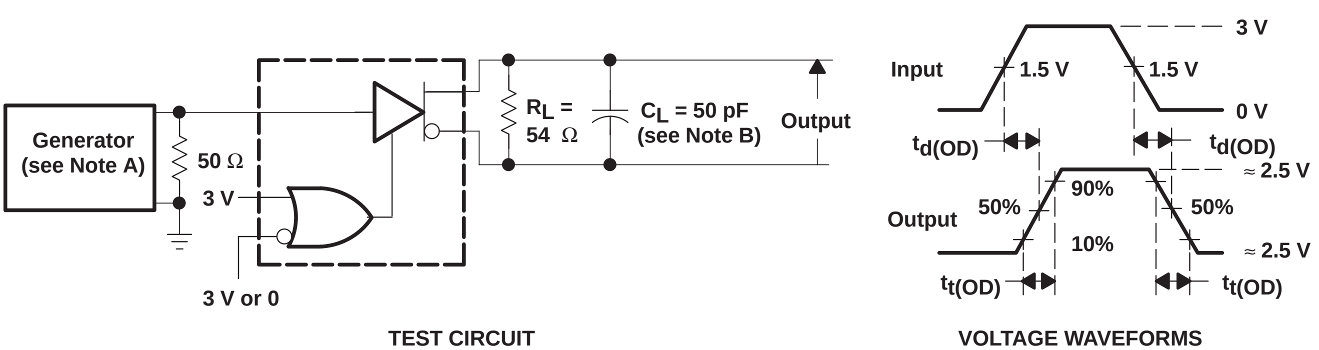


Figure 1. Differential and Common-Mode Output Voltages

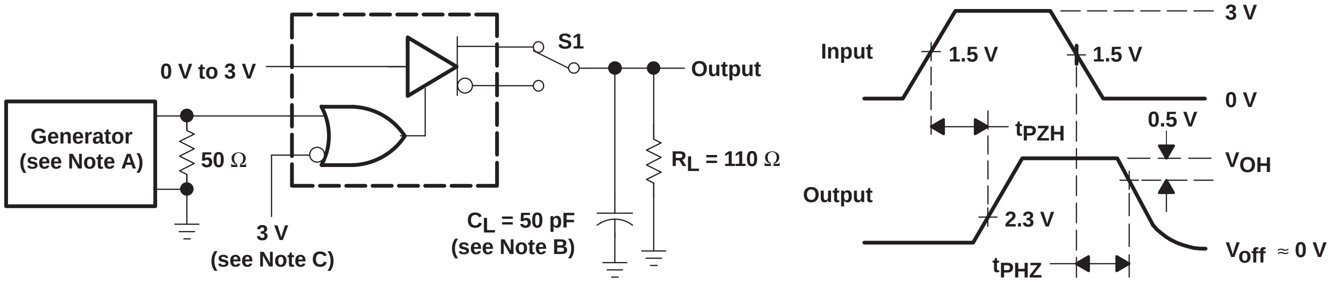


NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

Figure 2. Differential-Output Test CIrcuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

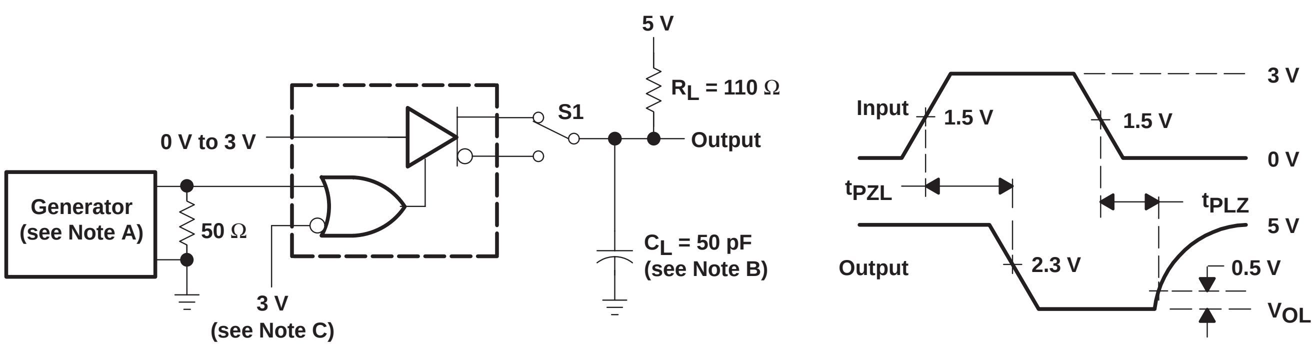
VOLTAGE WAVEFORMS

NOTES. A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50\ \Omega$.

B. C_L includes probe and stray capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 3. Test Circuit and Voltage Waveforms



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES. A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50\ \Omega$.

B. C_L includes probe and stray capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

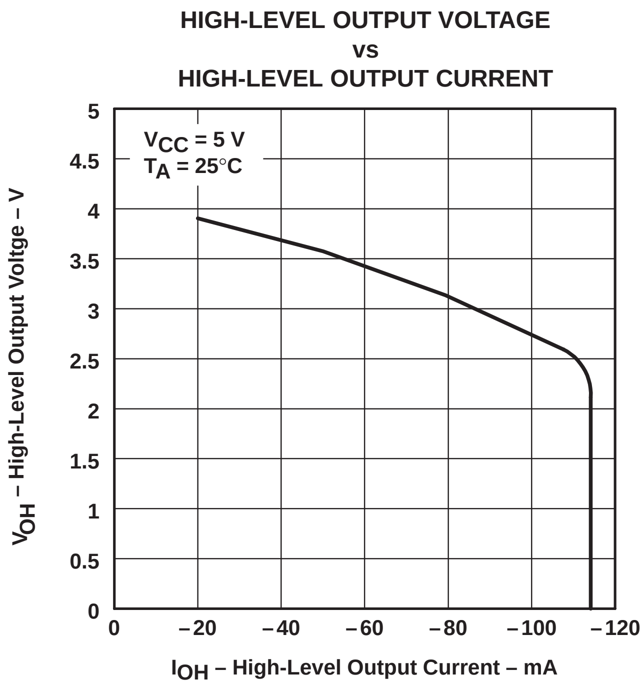


Figure 5

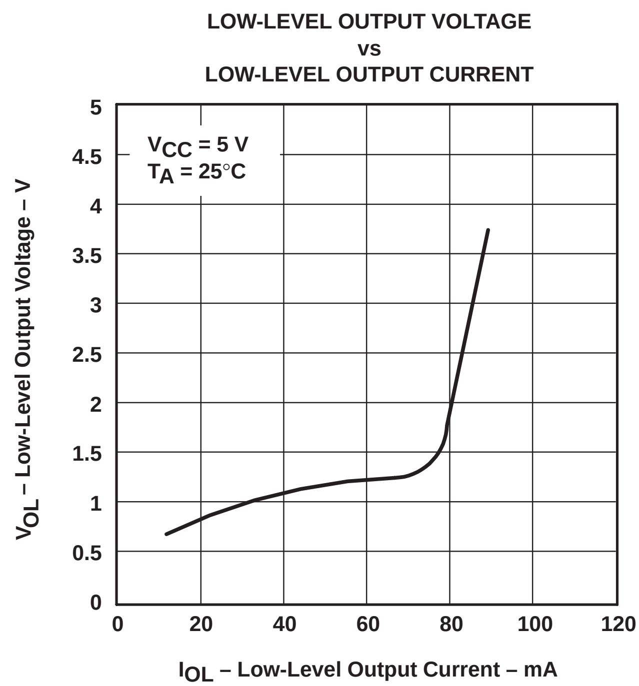


Figure 6

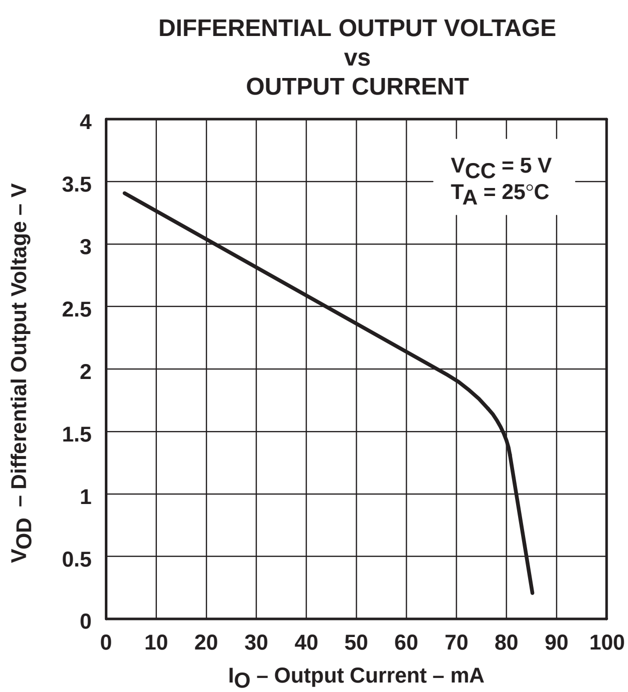


Figure 7

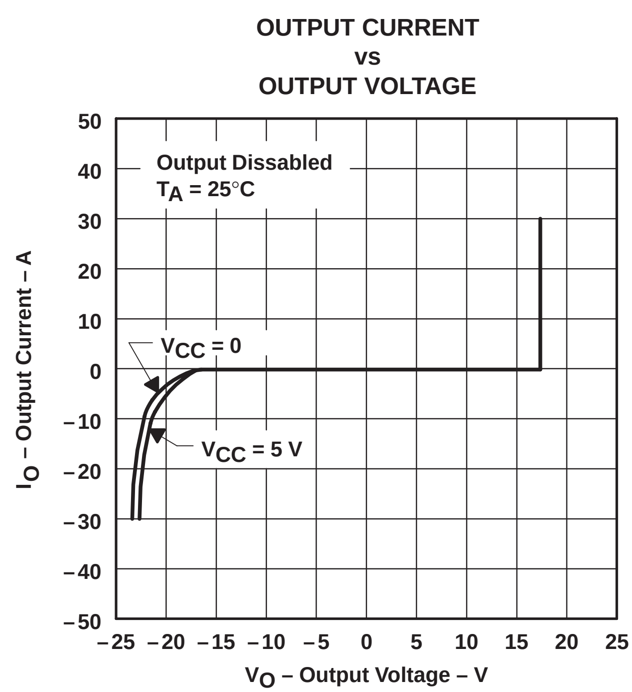


Figure 8

TYPICAL CHARACTERISTICS

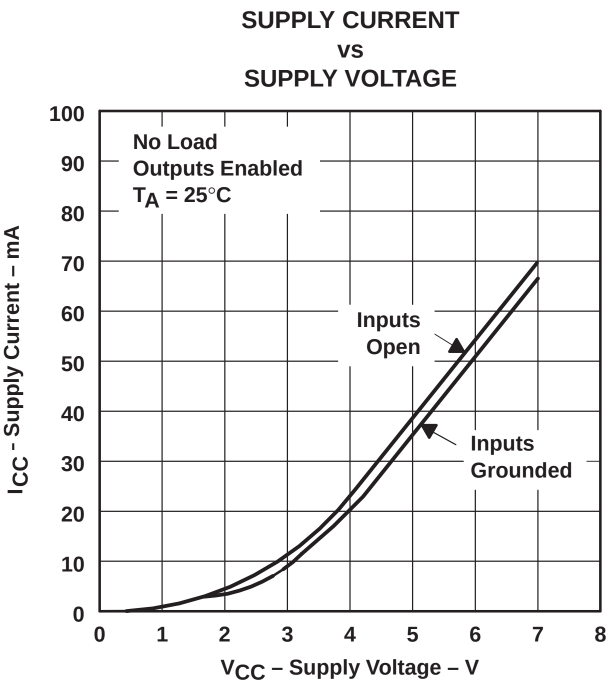


Figure 9

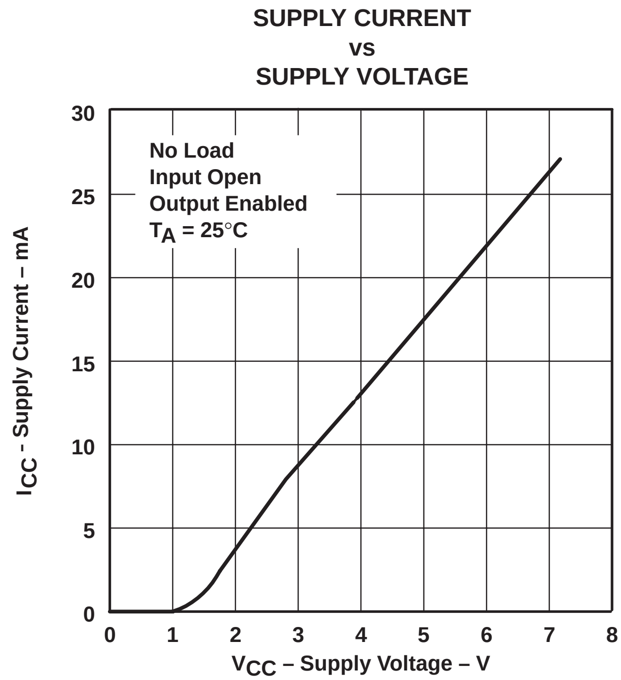
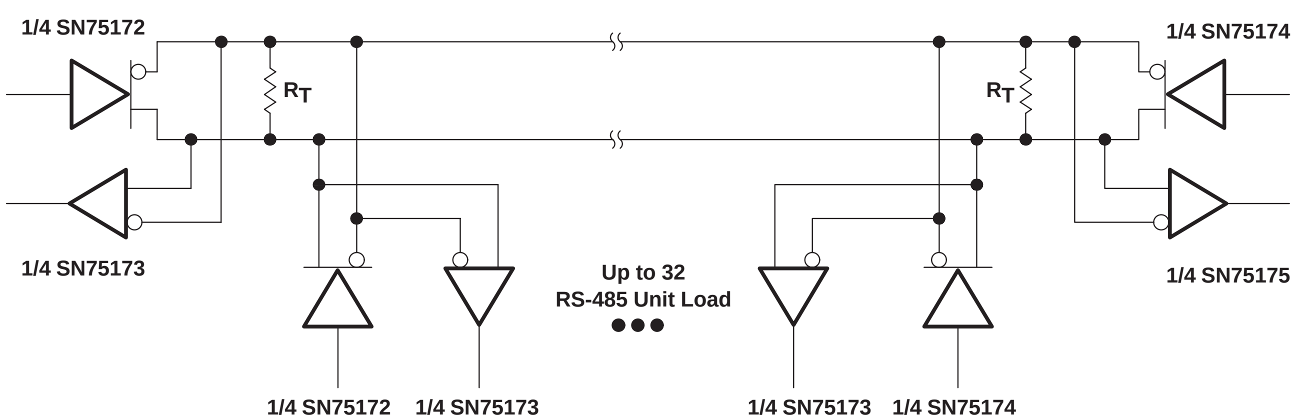


Figure 10

APPLICATION INFORMATION



NOTE A: The line length should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75172DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75172	Samples
SN75172DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75172	Samples
SN75172DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75172	Samples
SN75172DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75172	Samples
SN75172N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75172N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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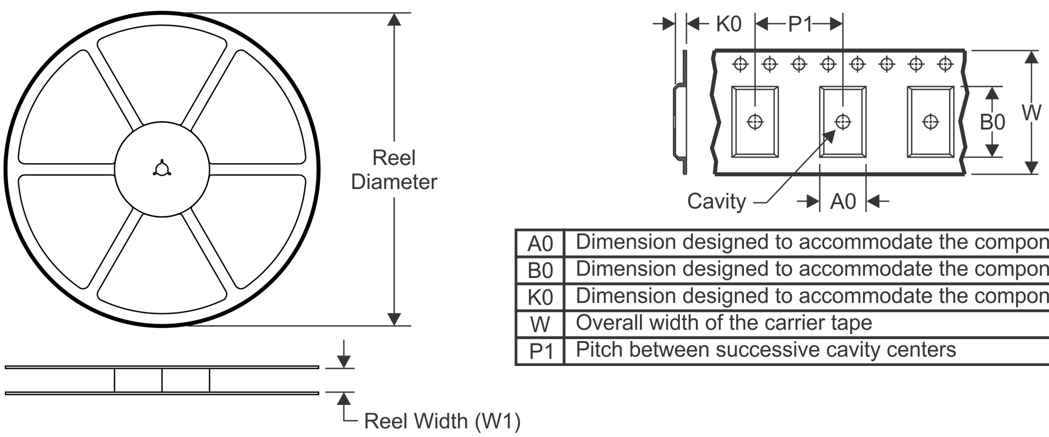
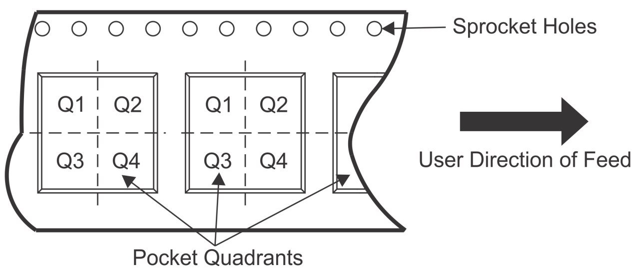
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

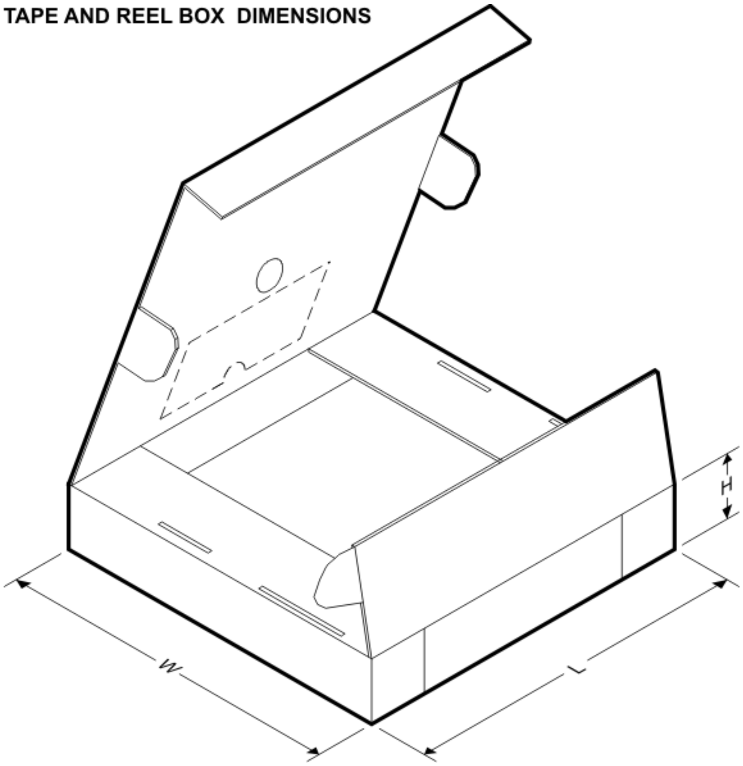
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

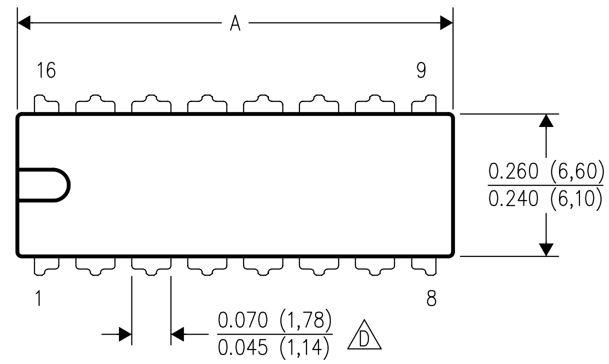


*All dimensions are nominal

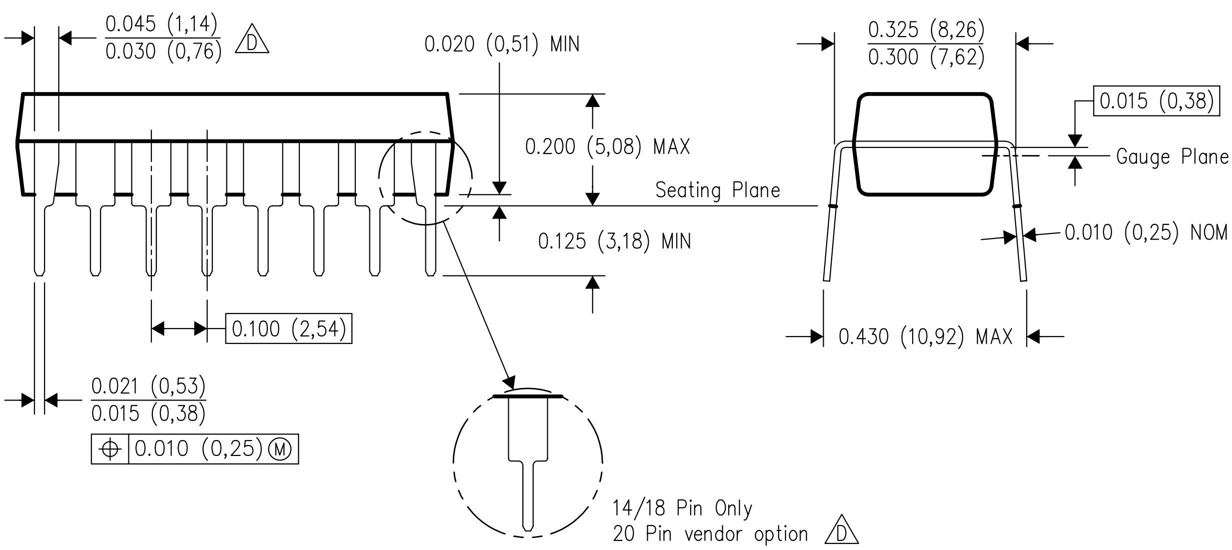
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75172DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75172DWR	SOIC	DW	20	2000	367.0	367.0	45.0

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



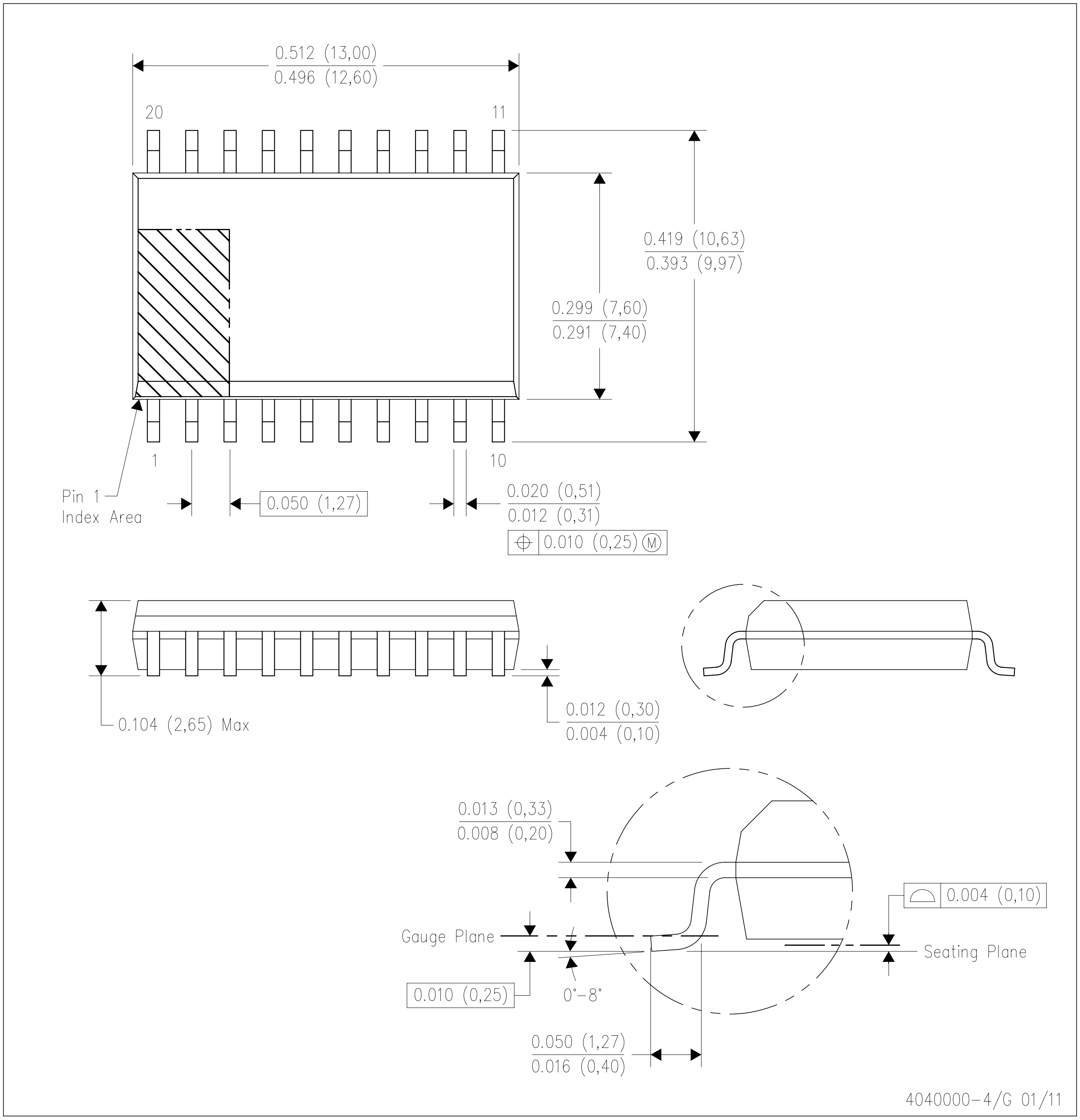
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

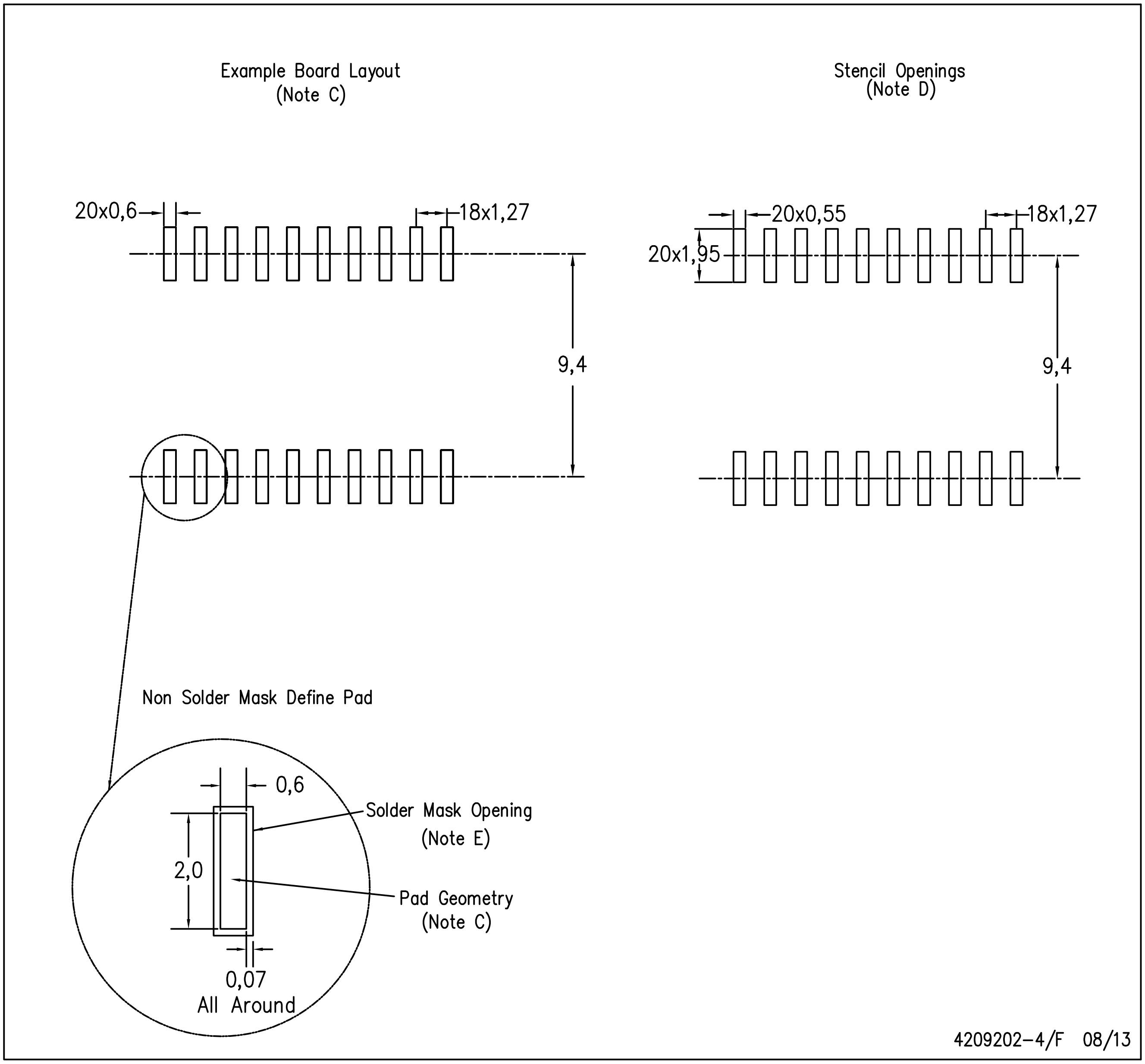
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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