

SN74LVC244A Octal Buffer/Driver With 3-State Outputs

1 Features

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Specified From -40°C to 85°C and -40°C to 125°C
- Max t_{pd} of 5.9 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Max of 5.5 V Down to the V_{CC} Level
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
 - 1000-V Charged-Device Model

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

3 Description

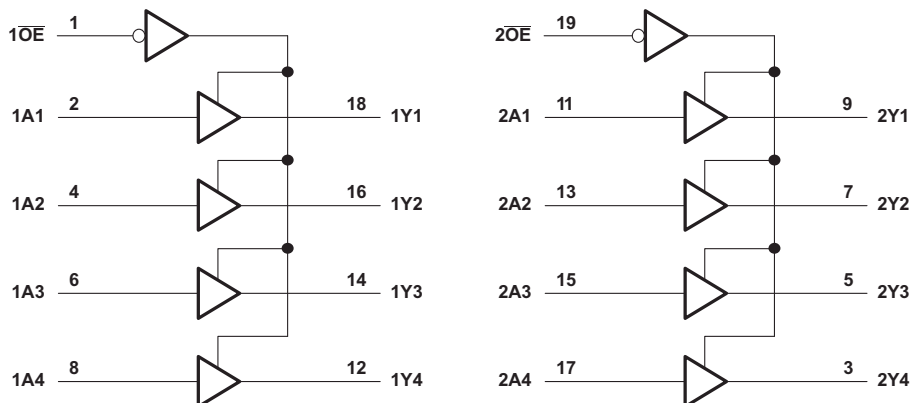
These octal bus buffers are designed for 1.65-V to 3.6-V V_{CC} operation. The 'LVC244A devices are designed for asynchronous communication between data buses.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE (PIN) | BODY SIZE |
|-------------|---------------|--------------------|
| SN74LVC244A | PDIP (20) | 25.40 mm x 6.35 mm |
| | SOP (20) | 12.60 mm x 5.30 mm |
| | SSOP (20) | 7.50 mm x 5.30 mm |
| | TVSOP (20) | 5.00 mm x 4.40 mm |
| | SOIC (20) | 12.80 mm x 7.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.



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5 Revision History

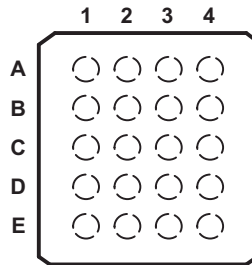
Changes from Revision Y (September 2010) to Revision Z

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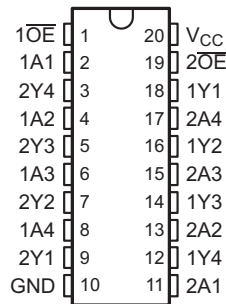
| | |
|--|----------|
| • Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. | 1 |
| • Deleted <i>Ordering Information</i> table. | 1 |
| • Updated <i>Features</i> | 1 |

6 Pin Configuration and Functions

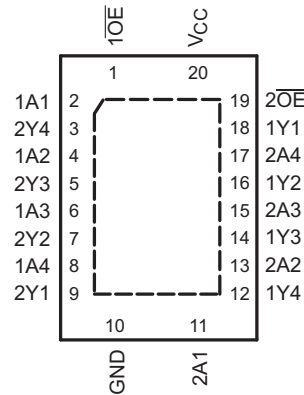
GQN OR ZQN PACKAGE
(TOP VIEW)



DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
|-----------------|------------------------------|------------|------|---------------|
| | DB, DGV, DW, NS, PW, and RGY | GQN or ZQN | | |
| 1A1 | 2 | A1 | I | Input |
| 1A2 | 4 | B1 | I | Input |
| 1A3 | 6 | C1 | I | Input |
| 1A4 | 8 | D1 | I | Input |
| 1OE | 1 | A2 | I | Output enable |
| 1Y1 | 18 | B4 | O | Output |
| 1Y2 | 16 | C4 | O | Output |
| 1Y3 | 14 | D4 | O | Output |
| 1Y4 | 12 | E4 | O | Output |
| 2A1 | 11 | E3 | I | Input |
| 2A2 | 13 | D2 | I | Input |
| 2A3 | 15 | C3 | I | Input |
| 2A4 | 17 | B2 | I | Input |
| 2OE | 19 | A2 | I | Output enable |
| 2Y1 | 9 | E2 | O | Output |
| 2Y2 | 7 | D3 | O | Output |
| 2Y3 | 5 | C2 | O | Output |
| 2Y4 | 3 | B3 | O | Output |
| GND | 10 | E1 | — | Ground |
| V _{CC} | 20 | A3 | — | Power pin |

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------|---|---|-----------------------|------|----|
| V _{CC} | Supply voltage range | -0.5 | 6.5 | V | |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V | |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V | |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V | |
| I _{IK} | Input clamp current | V _I < 0 | -50 | mA | |
| I _{OK} | Output clamp current | V _O < 0 | -50 | mA | |
| I _O | Continuous output current | | ±50 | mA | |
| | Continuous current through V _{CC} or GND | | ±100 | mA | |
| θ _{JA} | Package thermal impedance | DB package ⁽⁴⁾ | 70 | °C/W | |
| | | DGV package ⁽⁴⁾ | 92 | | |
| | | DW package ⁽⁴⁾ | 58 | | |
| | | GQN or ZQN package ⁽⁴⁾ | 78 | | |
| | | N package ⁽⁴⁾ | 69 | | |
| | | NS package ⁽⁴⁾ | 60 | | |
| | | PW package ⁽⁴⁾ | 83 | | |
| | | RGY package ⁽⁵⁾ | 37 | | |
| P _{tot} | Power dissipation | T _A = -40°C to 125°C ⁽⁶⁾⁽⁷⁾ | 500 | mW | |
| T _{stg} | Storage temperature range | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.
- (6) For the DW package: above 70°C the value of P_{tot} derates linearly with 8 mW/K.
- (7) For the DB, DGV, N, NS, and PW packages: above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

7.2 ESD Ratings

| PARAMETER | DEFINITION | VALUE | UNIT |
|--------------------|-------------------------|--|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 2000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | T _A = 25°C | | –40 TO 85°C | | –40 TO 125°C | | UNIT |
|-----------------|---------------------------|------------------------------------|-----------------|------------------------|-----------------|------------------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | Operating | | 1.65 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | | 1.5 | | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.65 × V _{CC} | | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 1.7 | | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | | 2 | | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | | 0.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | | 0.8 | | 0.8 | | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | | –4 | | mA |
| | | V _{CC} = 2.3 V | | –8 | | –8 | | |
| | | V _{CC} = 2.7 V | | –12 | | –12 | | |
| | | V _{CC} = 3 V | | –24 | | –24 | | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | | 4 | | mA |
| | | V _{CC} = 2.3 V | | 8 | | 8 | | |
| | | V _{CC} = 2.7 V | | 12 | | 12 | | |
| | | V _{CC} = 3 V | | 24 | | 24 | | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74LVC244A | | | | | | | | UNIT |
|-------------------------------|--|-------------------|--------------------|-------------------|---------------------------|------------------|-------------------|-------------------|--------------------|------|
| | | DB ⁽²⁾ | DGV ⁽²⁾ | DW ⁽²⁾ | GQN or ZQN ⁽²⁾ | N ⁽²⁾ | NS ⁽²⁾ | PW ⁽²⁾ | RGY ⁽³⁾ | |
| | | 20 PINS | | | | | | | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 108.1 | 128.7 | 90.9 | 78 | 61.6 | 90.1 | 114.7 | 50.3 | °C/W |
| R _{θJC(to p)} | Junction-to-case(top) thermal resistance | 70.2 | 43.7 | 55.3 | | 46.5 | 56.4 | 48.4 | 58.4 | |
| R _{θJB} | Junction-to-board thermal resistance | 63.3 | 70.2 | 58.8 | | 42.5 | 57.7 | 65.6 | 28.3 | |
| ψ _{JT} | Junction-to-top characterization parameter | 30.6 | 3.1 | 29.1 | | 34.6 | 28.4 | 6.8 | 4.9 | |
| ψ _{JB} | Junction-to-board characterization parameter | 62.9 | 69.5 | 58.3 | | 42.4 | 57.2 | 65.1 | 28.4 | |
| R _{θJC(to t)} | Junction-to-case(bottom) thermal resistance | — | — | — | | — | — | — | 22.7 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

(3) The package thermal impedance is calculated in accordance with JESD 51-5.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | –40 TO 85°C | | –40 TO 125°C | | UNIT |
|--------------------------|--|-----------------|-----------------------|-----|-----|-----------------------|-----|-----------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = –100 μA | 1.65 V to 3.6 V | V _{CC} – 0.2 | | | V _{CC} – 0.2 | | V _{CC} – 0.3 | | V |
| | I _{OH} = –4 mA | 1.65 V | 1.29 | | | 1.2 | | 1.05 | | |
| | I _{OH} = –8 mA | 2.3 V | 1.9 | | | 1.7 | | 1.55 | | |
| | I _{OH} = –12 mA | 2.7 V | 2.2 | | | 2.2 | | 2.05 | | |
| | | 3 V | 2.4 | | | 2.4 | | 2.25 | | |
| I _{OH} = –24 mA | 3 V | 2.3 | | | 2.2 | | 2 | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | 0.1 | | | 0.2 | | 0.3 | | V |
| | I _{OL} = 4 mA | 1.65 V | 0.24 | | | 0.45 | | 0.6 | | |
| | I _{OL} = 8 mA | 2.3 V | 0.3 | | | 0.7 | | 0.75 | | |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | | 0.4 | | 0.6 | | |
| | I _{OL} = 24 mA | 3 V | 0.55 | | | 0.55 | | 0.8 | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | ±1 | | | ±5 | | ±20 | | μA |
| I _{off} | V _I or V _O = 5.5 V | 0 | ±1 | | | ±10 | | ±20 | | μA |
| I _{OZ} | V _O = 0 to 5.5 V | 3.6 V | ±1 | | | ±10 | | ±20 | | μA |
| I _{CC} | V _I = V _{CC} or GND | 3.6 V | 1 | | | 10 | | 40 | | μA |
| | 3.6 V ≤ V _I ≤ 5.5 V ⁽¹⁾ | | 1 | | | 10 | | 40 | | |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | 500 | | | 500 | | 5000 | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 4 | | | | | | | pF |
| C _o | V _O = V _{CC} or GND | 3.3 V | 5.5 | | | | | | | pF |

(1) This applies in the disabled state only.

7.6 Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

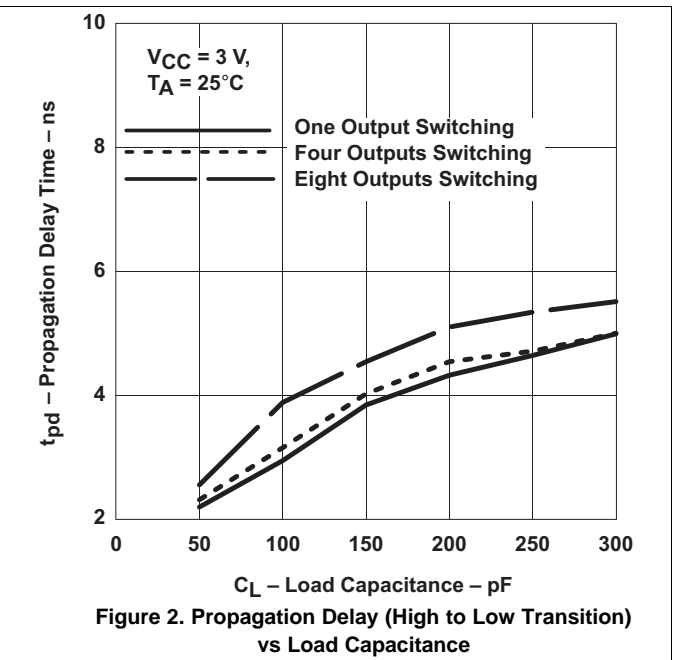
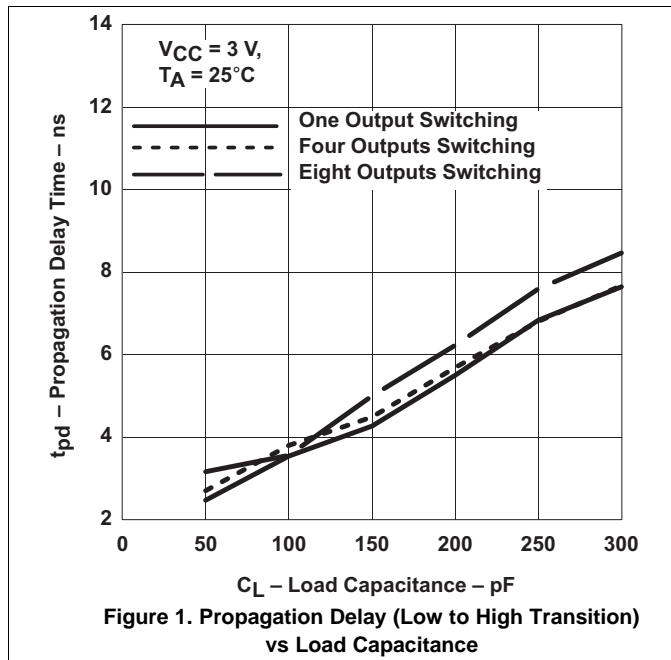
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | –40 TO 85°C | | –40 TO 125°C | | UNIT |
|--------------------|------------------------|-------------|-----------------|-----------------------|-----|------|-------------|------|--------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 1.5 V | 1 | 7 | 14.4 | 1 | 14.9 | 1 | 16.4 | ns |
| | | | 1.8 V ± 0.15 V | 1 | 5.9 | 10.4 | 1 | 10.9 | 1 | 12.4 | |
| | | | 2.5 V ± 0.2 V | 1 | 4.2 | 7.4 | 1 | 7.9 | 1 | 10 | |
| | | | 2.7 V | 1 | 4.2 | 6.7 | 1 | 6.9 | 1 | 8.2 | |
| | | | 3.3 V ± 0.3 V | 1.5 | 3.9 | 5.7 | 1.5 | 5.9 | 1.5 | 7.2 | |
| t _{en} | $\overline{\text{OE}}$ | Y | 1.5 V | 1 | 8.3 | 17.8 | 1 | 18.3 | 1 | 19.8 | ns |
| | | | 1.8 V ± 0.15 V | 1 | 6.4 | 12.1 | 1 | 12.6 | 1 | 14.1 | |
| | | | 2.5 V ± 0.2 V | 1 | 4.6 | 9.1 | 1 | 9.6 | 1 | 11.7 | |
| | | | 2.7 V | 1 | 5 | 8.4 | 1 | 8.6 | 1 | 10.3 | |
| | | | 3.3 V ± 0.3 V | 1.5 | 4.5 | 7.4 | 1.5 | 7.6 | 1.5 | 9.4 | |
| t _{dis} | $\overline{\text{OE}}$ | Y | 1.5 V | 1 | 7.2 | 15.6 | 1 | 16.1 | 1 | 17.6 | ns |
| | | | 1.8 V ± 0.15 V | 1 | 5.8 | 11.6 | 1 | 12.1 | 1 | 13.6 | |
| | | | 2.5 V ± 0.2 V | 1 | 3.7 | 7.3 | 1 | 7.8 | 1 | 9.9 | |
| | | | 2.7 V | 1 | 3.8 | 6.6 | 1 | 6.8 | 1 | 8.6 | |
| | | | 3.3 V ± 0.3 V | 1.5 | 3.8 | 6.3 | 1.5 | 6.5 | 1.5 | 8 | |
| t _{sk(o)} | | | 3.3 V ± 0.3 V | | | | 1 | | 1.5 | ns | |

7.7 Operating Characteristics

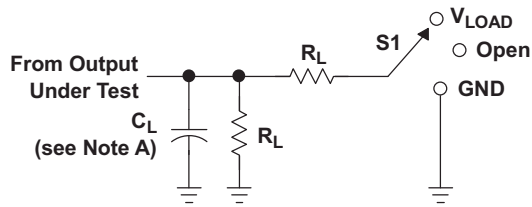
T_A = 25°C

| PARAMETER | | TEST CONDITIONS | V _{CC} | TYP | UNIT | |
|-----------------|---|-----------------|-----------------|-------|------|----|
| C _{pd} | Power dissipation capacitance per buffer/driver | Outputs enabled | f = 10 MHz | 1.8 V | 43 | pF |
| | | | | 2.5 V | 43 | |
| | | | | 3.3 V | 44 | |
| | Outputs disabled | f = 10 MHz | 1.8 V | 1 | | |
| | | | 2.5 V | 1 | | |
| | | | 3.3 V | 2 | | |

7.8 Typical Characteristics

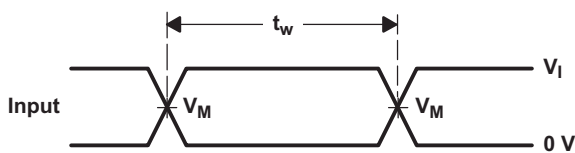
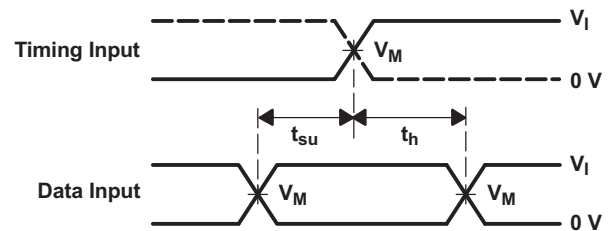
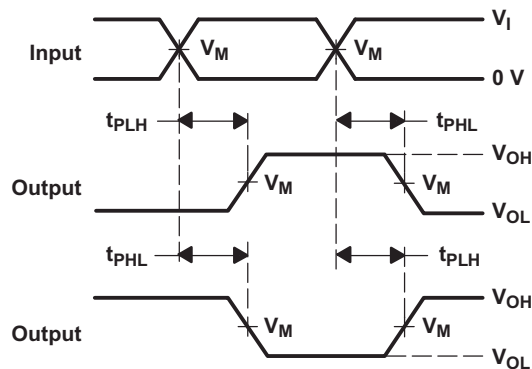
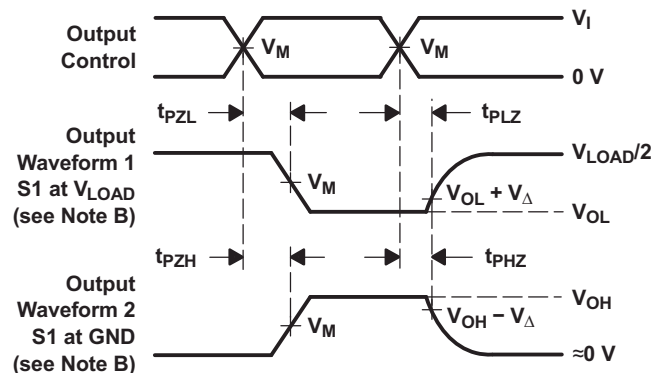


8 Parameter Measurement Information


LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|--------------------|----------|---------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| 1.5 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 2 k Ω | 0.1 V |
| 1.8 V \pm 0.15 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| 2.5 V \pm 0.2 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V \pm 0.3 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |


**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

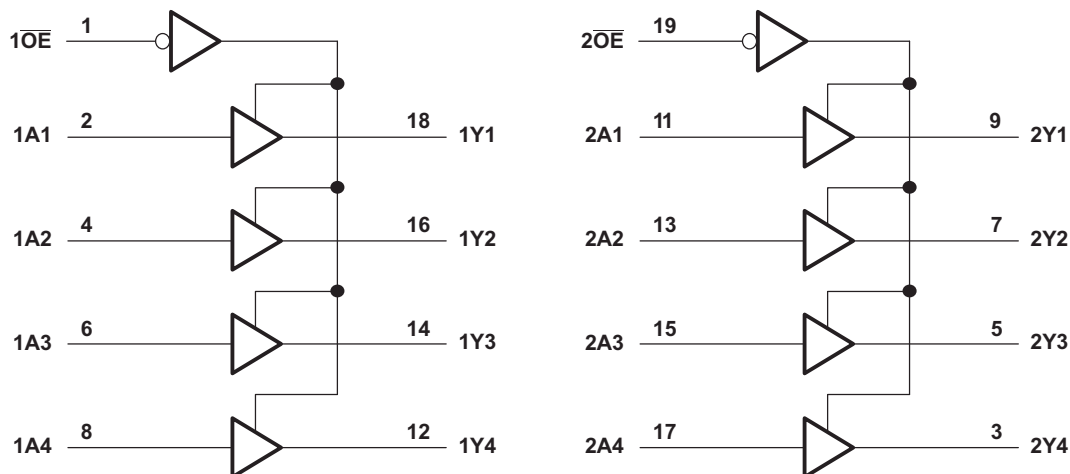
Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The LVC244A device is organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

9.2 Functional Block Diagram



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.

9.3 Feature Description

- Allows down voltage translation
 - 5 V to 3.3 V
 - 5 V or 3.3 V to 1.8 V
- Inputs accept voltage levels up to 5.5 V

9.4 Device Functional Modes

Table 1. Function Table

| INPUTS | | OUTPUT Y |
|-----------------|---|-------------|
| \overline{OE} | A | |
| L | H | H |
| L | L | L |
| H | X | Z |

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

SN74LVC244A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it ideal for down translation.

10.2 Typical Application

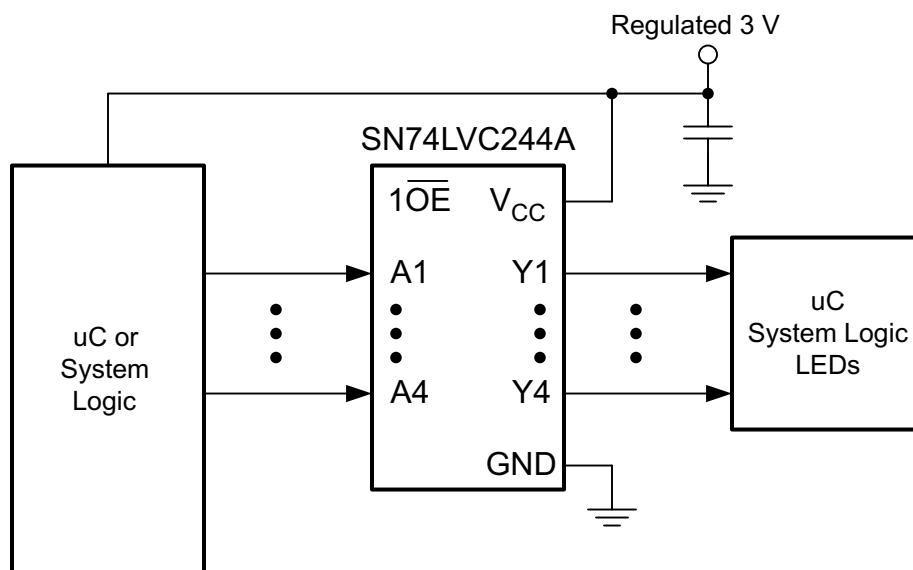


Figure 4. Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:

- For rise time and fall time specifications, see $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
- For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the [Recommended Operating Conditions](#) table at any valid V_{CC} .

2. Recommend Output Conditions:

- Load currents should not exceed $(I_O \text{ max})$ per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
- Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves

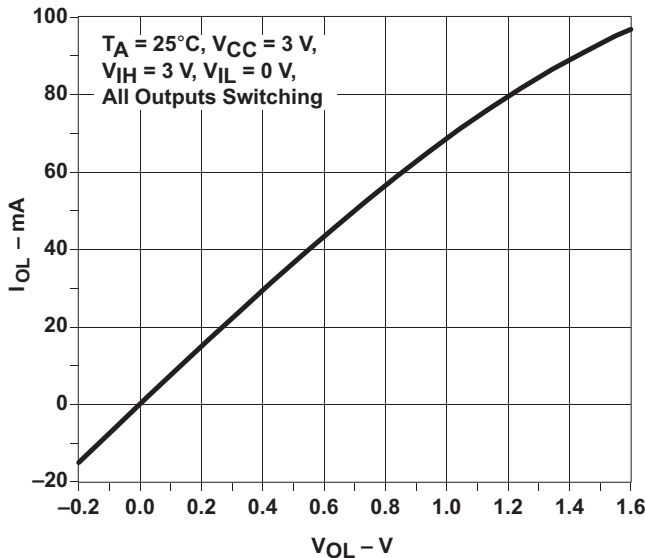


Figure 5. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

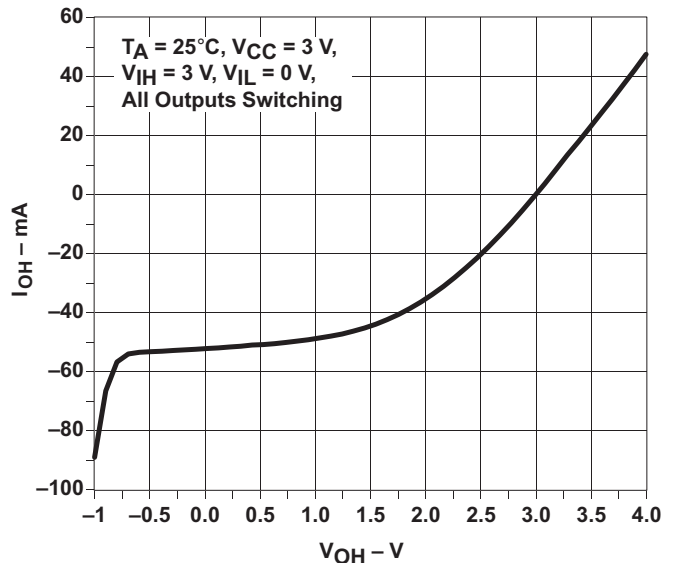


Figure 6. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

12.2 Layout Example

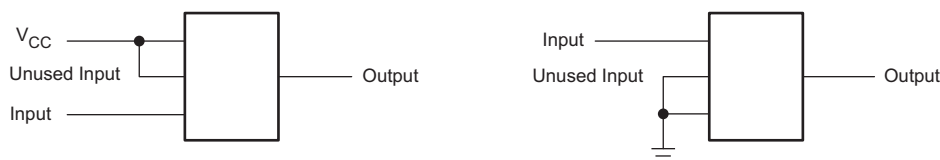


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|----------------------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC244ADBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI | -40 to 125 | | |
| SN74LVC244ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244ADBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244ADGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244ADGVRE4 | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244ADGVRG4 | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC244A | Samples |
| SN74LVC244ADWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC244A | Samples |
| SN74LVC244ADWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC244A | Samples |
| SN74LVC244ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | LVC244A | Samples |
| SN74LVC244ADWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC244A | Samples |
| SN74LVC244ADWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC244A | Samples |
| SN74LVC244AGQNR | OBSOLETE | BGA MICROSTAR JUNIOR | GQN | 20 | | TBD | Call TI | Call TI | -40 to 85 | LC244A | |
| SN74LVC244AN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | SN74LVC244AN | Samples |
| SN74LVC244ANE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | SN74LVC244AN | Samples |
| SN74LVC244ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC244A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|----------------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC244ANSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC244A | Samples |
| SN74LVC244APW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244APWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244APWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244APWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 125 | | |
| SN74LVC244APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244APWRG3 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244APWT | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244APWTE4 | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244APWTG4 | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC244A | Samples |
| SN74LVC244ARGYR | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC244A | Samples |
| SN74LVC244ARGYRG4 | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC244A | Samples |
| SN74LVC244AZQNR | ACTIVE | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | LC244A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC244A :

- Automotive: [SN74LVC244A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC244ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC244ADGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC244ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVC244ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 4.0 | 24.0 | Q1 |
| SN74LVC244APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC244APWRG3 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC244APWT | TSSOP | PW | 20 | 250 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC244ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC244ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC244AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC244ADBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC244ADGVR | TVSOP | DGV | 20 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC244ADWR | SOIC | DW | 20 | 2000 | 366.0 | 364.0 | 50.0 |
| SN74LVC244ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC244APWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC244APWRG3 | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LVC244APWT | TSSOP | PW | 20 | 250 | 367.0 | 367.0 | 38.0 |
| SN74LVC244ARGYR | VQFN | RGY | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| SN74LVC244ARGYR | VQFN | RGY | 20 | 3000 | 355.0 | 350.0 | 50.0 |
| SN74LVC244AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 338.1 | 338.1 | 20.6 |

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



4200704/F 06/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BC-2.
 - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BC-2.
 - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

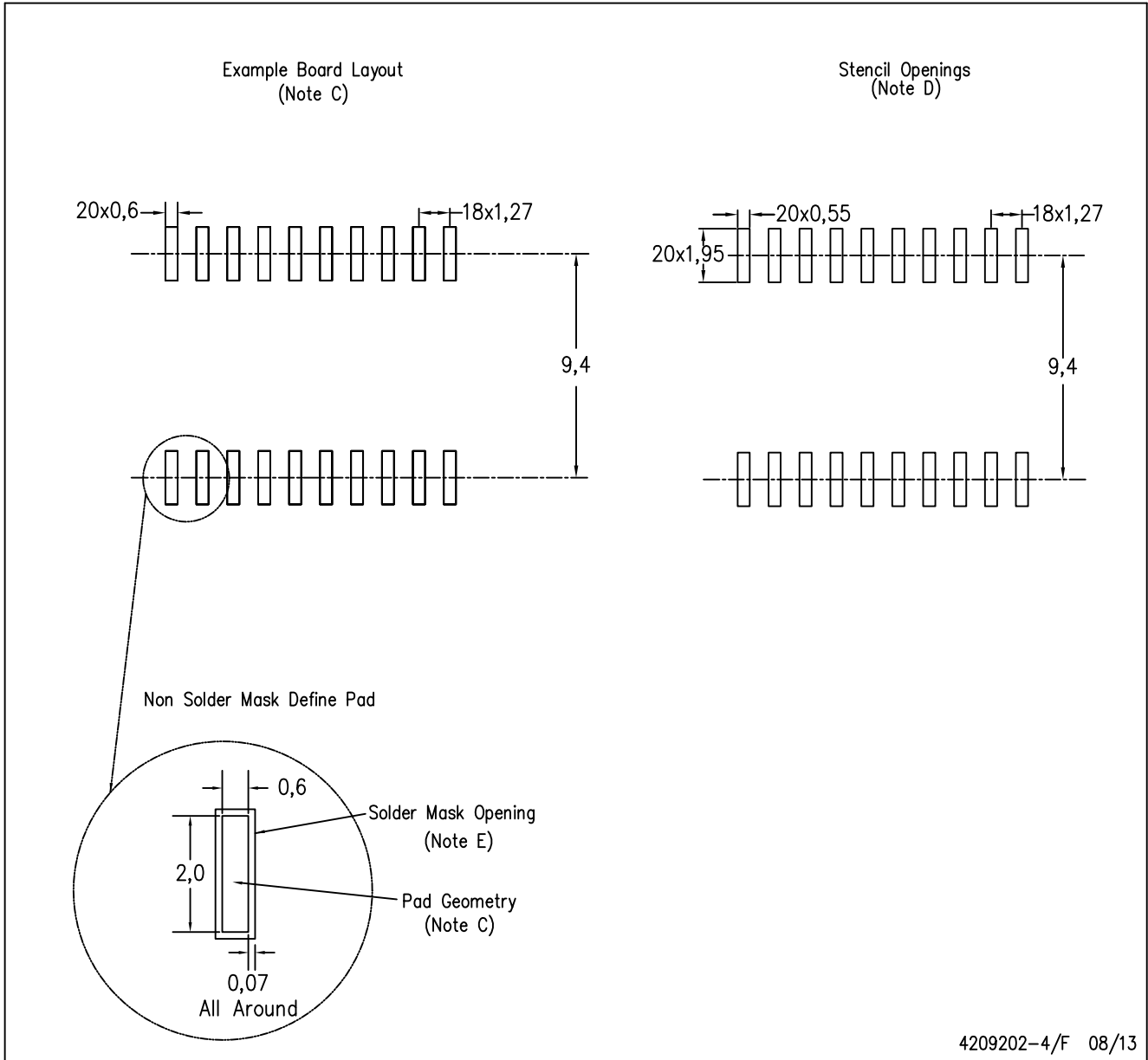
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

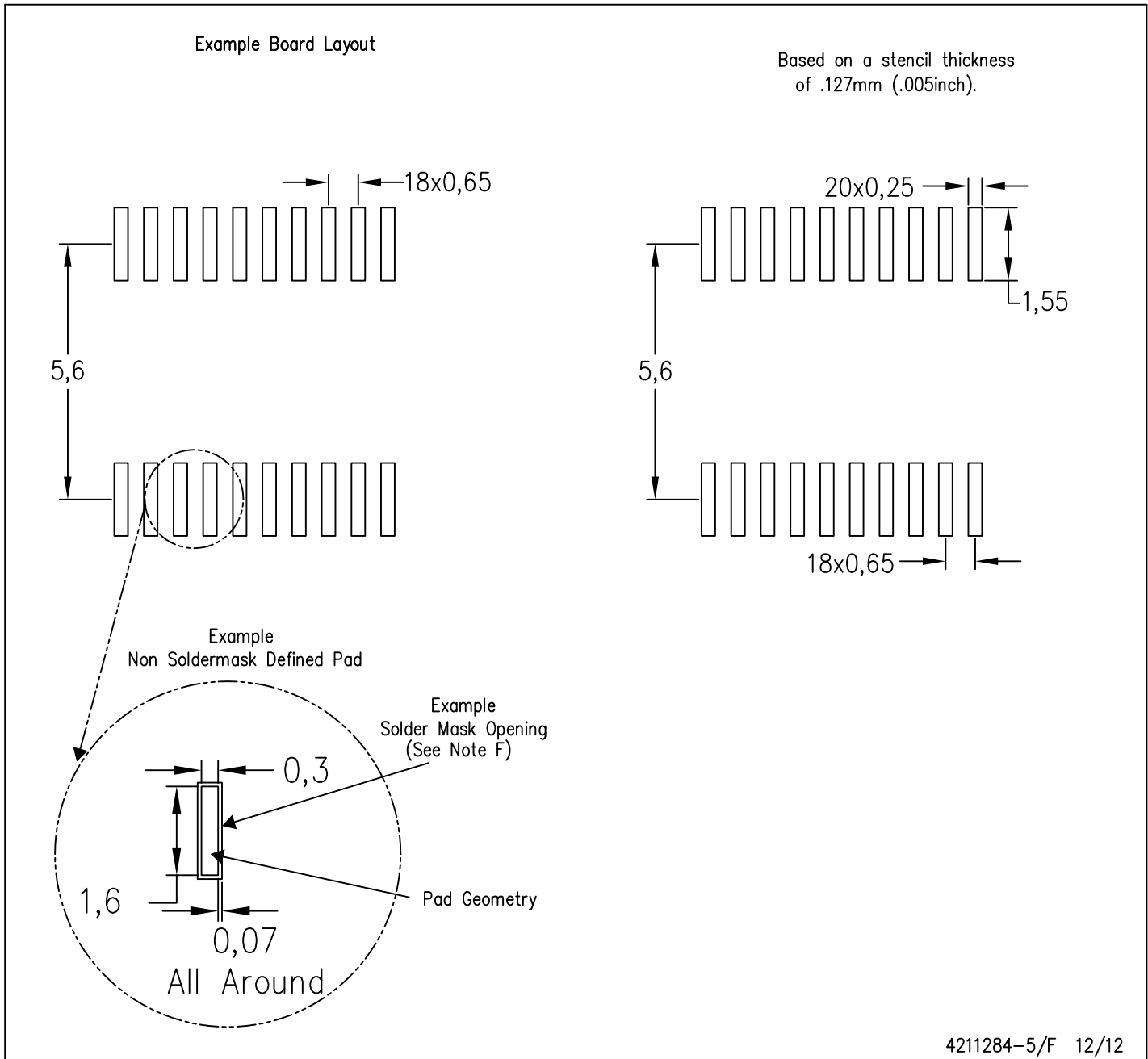


4209202-4/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-4/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-4/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-4/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

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| | |
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