

SNx4AHC540 Octal Buffers/Drivers With 3-State Outputs

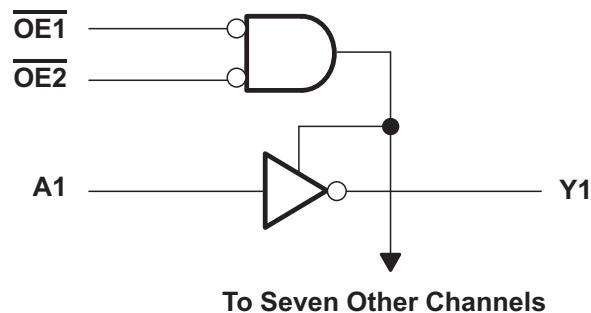
1 Features

- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Fitness Devices
- Telecom Infrastructures
- Electronic Points of Sale

4 Simplified Schematic



3 Description

The SNx4AHC540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC540	PDIP (20)	25.40 mm x 6.35 mm
	SSOP (20)	7.50 mm x 5.30 mm
	TSSOP (20)	6.50 mm x 4.40 mm
	TVSOP (20)	5.00 mm x 4.40 mm
	SOIC (20)	12.80 mm x 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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5 Revision History

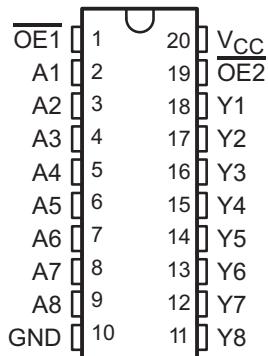
Changes from Revision J (July 2003) to Revision K

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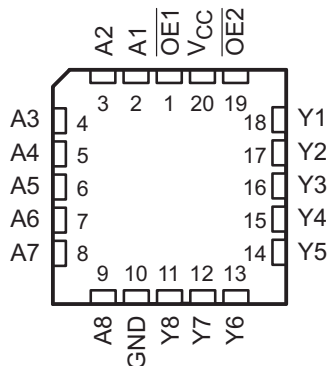
• Updated document to new TI data sheet format	1
• Deleted Ordering Information table	1
• Added Military Disclaimer to Features list	1
• Added Applications	1
• Added Pin Functions table	3
• Added Handling Ratings table	4
• Extended operating temperature range to 125°C	4
• Added Thermal Information table	5
• Added –40°C to 125°C range for SN74AHC540 in Electrical Characteristics table	5
• Added $T_A = -40^\circ\text{C}$ to 125°C for SN74AHC540 in both Switching Characteristics tables	6
• Added Typical Characteristics	7
• Added Detailed Description section	9
• Added Application and Implementation section	10
• Added Power Supply Recommendations and Layout sections	11

6 Pin Configuration and Functions

SN54AHC540 . . . J OR W PACKAGE
SN74AHC540 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC540 . . . FK PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{OE1}$	I	Output Enable 1
2	A1	I	A1 Input
3	A2	I	A2 Input
4	A3	I	A3 Input
5	A4	I	A4 Input
6	A5	I	A5 Input
7	A6	I	A6 Input
8	A7	I	A7 Input
9	A8	I	A8 Input
10	GND	—	Ground
11	Y8	O	Y8 Output
12	Y7	O	Y7 Output
13	Y6	O	Y6 Output
14	Y5	O	Y5 Output
15	Y4	O	Y4 Output
16	Y3	O	Y3 Output
17	Y2	O	Y2 Output
18	Y1	O	Y1 Output
19	$\overline{OE2}$	I	Output Enable 2
20	V _{CC}	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-20 mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}		±20 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25 mA
Continuous current through V _{CC} or GND				±75 mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	-65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		
		0	1000	
		0	2000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AHC540		SN74AHC540		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5		V
		V _{CC} = 3 V		2.1		
		V _{CC} = 5.5 V		3.85		
V _{IL}	Low-level Input voltage	V _{CC} = 2 V		0.5		V
		V _{CC} = 3 V		0.9		
		V _{CC} = 5.5 V		1.65		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50		μA
		V _{CC} = 3.3 V ± 0.3 V		-4		mA
		V _{CC} = 5 V ± 0.5 V		-8		
I _{OL}	Low-level output current	V _{CC} = 2 V		50		μA
		V _{CC} = 3.3 V ± 0.3 V		4		mA
		V _{CC} = 5 V ± 0.5 V		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		ns/V
		V _{CC} = 5 V ± 0.5 V		20		
T _A	Operating free-air temperature	-55	125	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AHC540						UNIT
	DB	DGV	DW	N	NS	PW	
	20 PINS						
R _{θJA} Junction-to-ambient thermal resistance	99.9	119.2	83.0	54.9	80.4	105.4	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	61.7	34.5	48.9	41.7	46.9	39.5	
R _{θJB} Junction-to-board thermal resistance	55.2	60.7	50.5	35.8	47.9	56.4	
Ψ _{JT} Junction-to-top characterization parameter	22.6	1.2	21.1	27.9	19.9	3.1	
Ψ _{JB} Junction-to-board characterization parameter	54.8	60.0	50.1	35.7	47.5	55.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC540		SN74AHC540		–40°C to 125°C SN74AHC540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	2 V	1.9	2	1.9	1.9	1.9	1.9	1.9	1.9	V	
		3 V	2.9	3	2.9	2.9	2.9	2.9	2.9			
		4.5 V	4.4	4.5	4.4	4.4	4.4	4.4	4.4			
	I _{OH} = –4 mA	3 V	2.58		2.48	2.48	2.48	2.48	2.48			
	I _{OH} = –8 mA	4.5 V	3.94		3.8	3.8	3.8	3.8	3.8			
V _{OL}	I _{OL} = 50 μA	2 V		0.1	0.1	0.1	0.1	0.1	0.1	0.1	V	
		3 V		0.1	0.1	0.1	0.1	0.1	0.1			
		4.5 V		0.1	0.1	0.1	0.1	0.1	0.1			
	I _{OH} = 4 mA	3 V		0.36	0.5	0.44	0.44	0.44	0.44			
	I _{OH} = 8 mA	4.5 V		0.36	0.5	0.44	0.44	0.44	0.44			
I _I	V _I = 5.5 V or GND	0 V to 5.5 V		±0.1	±1 ⁽¹⁾	±1	±1	±1	±1	μA		
I _{OZ} ⁽²⁾	V _O = V _{CC} or GND V _I (OE) = V _{IL} or V _{IH}	5.5 V		±0.25	±2.5	±2.5	±2.5	±2.5	±2.5	μA		
I _{CC}	V _I = V _{CC} or GND I _O = 0	5.5 V		4	40	40	40	40	40	μA		
C _i	V _I = V _{CC} or GND	5 V		2	10		10			pF		
C _O	V _O = V _{CC} or GND	5 V		4						pF		

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) For input and output pins, I_{OZ} includes the input leakage current.

7.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		SN54AHC540		SN74AHC540		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$ SN74AHC540		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	4.8 ⁽¹⁾	7 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	9.5	ns
t_{PHL}				4.8 ⁽¹⁾	7 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	9.5	
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	6.8 ⁽¹⁾	10.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	1	13.5	ns
t_{PZL}				6.8 ⁽¹⁾	10.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	1	13.5	
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	6.8 ⁽¹⁾	10.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	1	13.5	ns
t_{PLZ}				6.8 ⁽¹⁾	10.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	1	13.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	7.3	10.5	1	12	1	12	1	13.5	ns
t_{PHL}				7.3	10.5	1	12	1	12	1	13.5	
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	8	14	1	16	1	16	1	17	ns
t_{PZL}				8	14	1	16	1	16	1	17	
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	8	15.4	1	17.5	1	17.5	1	18.5	ns
t_{PLZ}				8	15.4	1	17.5	1	17.5	1	18.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1.5 ⁽²⁾				1.5			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		SN54AHC540		SN74AHC540		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$ SN74AHC540		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.7 ⁽¹⁾	5 ⁽¹⁾	1 ⁽¹⁾	6 ⁽¹⁾	1	6	1	7	ns
t_{PHL}				3.7 ⁽¹⁾	5 ⁽¹⁾	1 ⁽¹⁾	6 ⁽¹⁾	1	6	1	7	
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.7 ⁽¹⁾	7.2 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	9.5	ns
t_{PZL}				4.7 ⁽¹⁾	7.2 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	9.5	
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.5 ⁽¹⁾	6.8 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	8.5	ns
t_{PLZ}				4.5 ⁽¹⁾	6.8 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	8.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.2	7	1	8	1	8	1	9	ns
t_{PHL}				5.2	7	1	8	1	8	1	9	
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.2	9.2	1	10.5	1	10.5	1	11.5	ns
t_{PZL}				6.2	9.2	1	10.5	1	10.5	1	11.5	
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6	8.8	1	10	1	10	1	10.5	ns
t_{PLZ}				6	8.8	1	10	1	10	1	10.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1 ⁽²⁾				1			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}^{(1)}$

PARAMETER		SN74AHC540		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

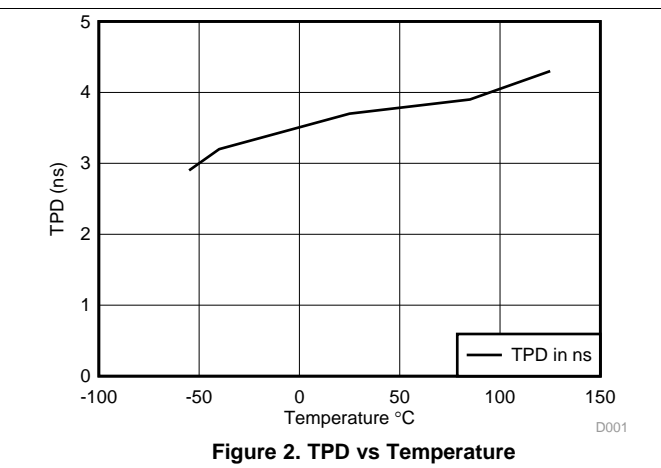
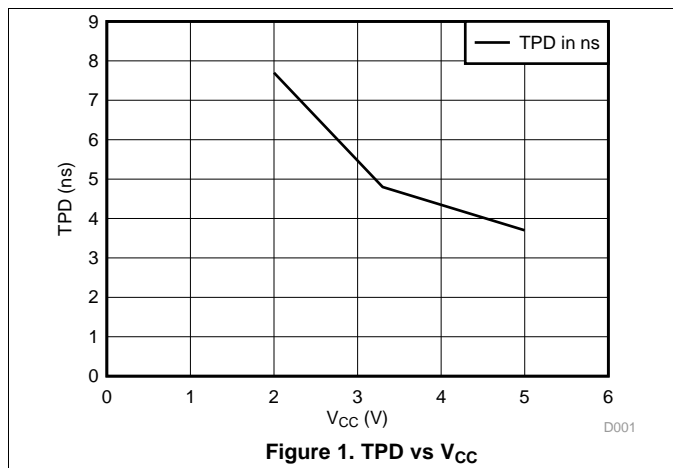
(1) Characteristics are for surface-mount packages only.

7.9 Operating Characteristics

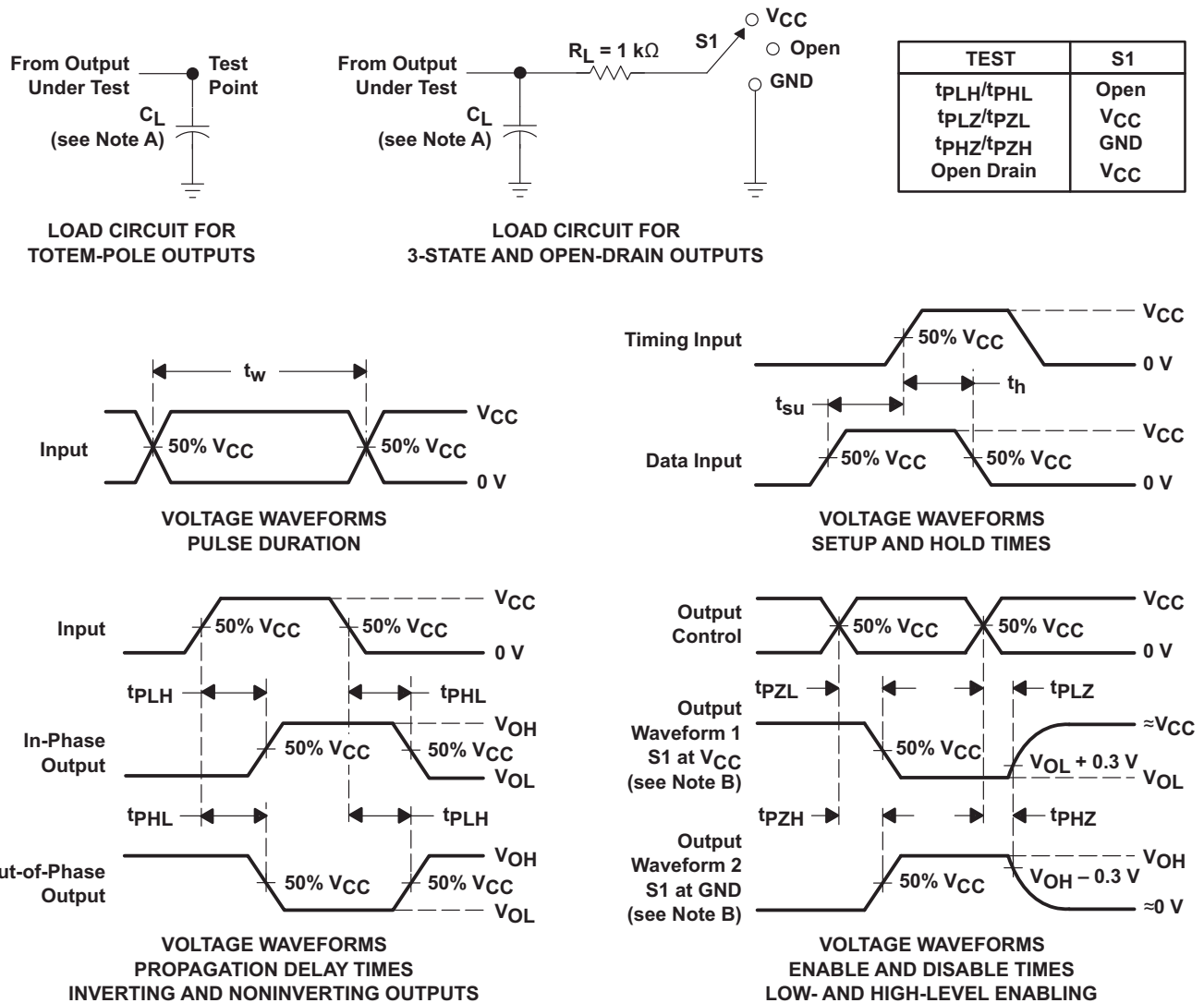
$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	No load, $f = 1\text{ MHz}$	12	pF

7.10 Typical Characteristics



8 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

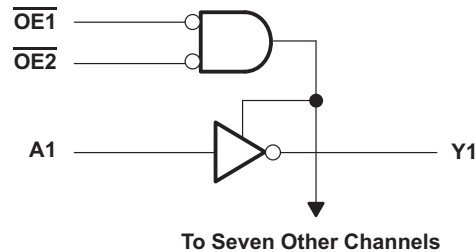
9.1 Overview

The SNx4AHC540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

9.2 Functional Block Diagram



9.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down voltage translation
 - Inputs accept voltages up to 5.5 V
- Slow edges reduce output ringing

9.4 Device Functional Modes

**Table 1. Function Table
(Each Buffer/Driver)**

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AHC540 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V, which allows down translation to the V_{CC} level. [Figure 5](#) shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

10.2 Typical Application

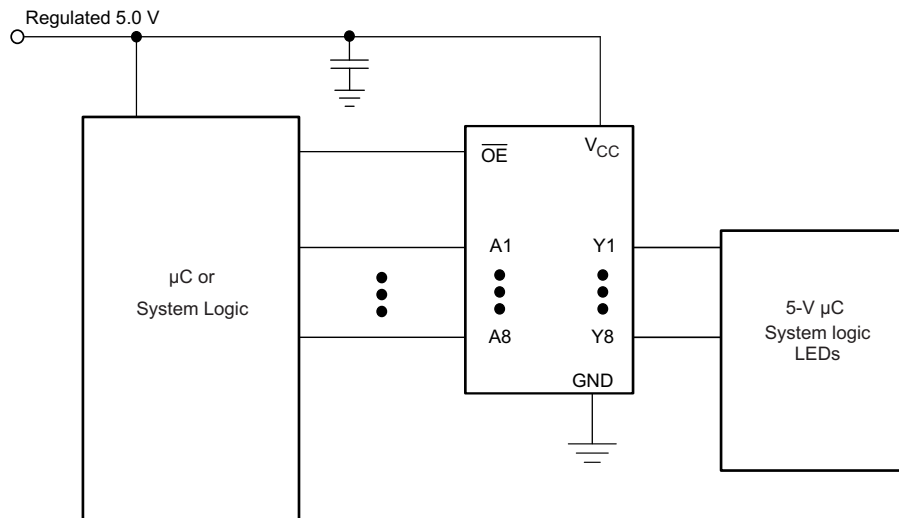


Figure 4. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommended Output Conditions:
 - Load currents should not exceed 25 mA per output and 75 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves

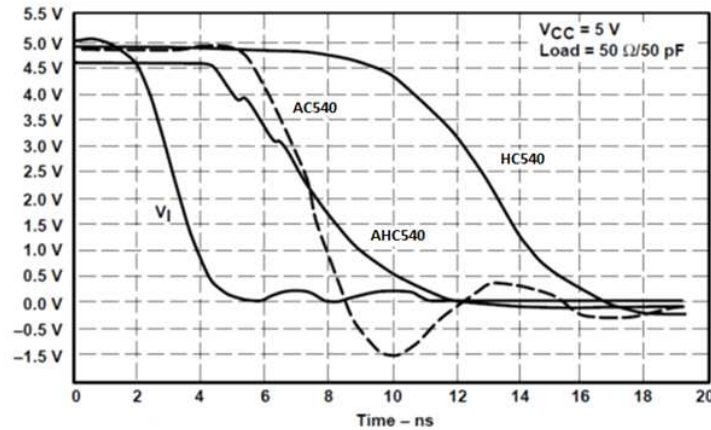


Figure 5. Switching Characteristics Comparison

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

12.2 Layout Example

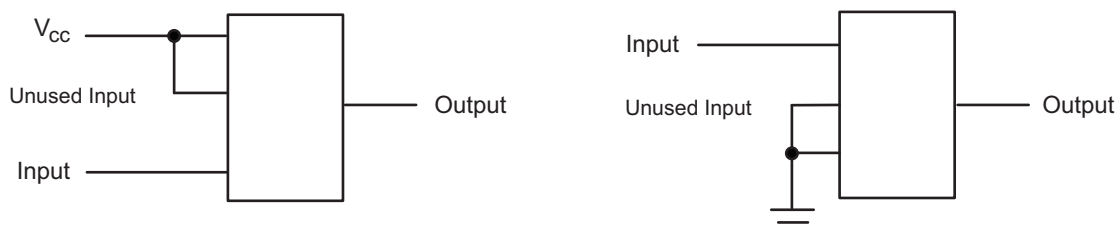


Figure 6. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC540	Click here	Click here	Click here	Click here	Click here
SN74AHC540	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9685001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9685001Q2A SNJ54AHC 540FK	Samples
5962-9685001QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685001QR A SNJ54AHC540J	Samples
5962-9685001QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685001QS A SNJ54AHC540W	Samples
SN74AHC540DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74AHC540DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540	Samples
SN74AHC540DGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540	Samples
SN74AHC540DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC540	Samples
SN74AHC540DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC540	Samples
SN74AHC540DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC540	Samples
SN74AHC540DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC540	Samples
SN74AHC540N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC540N	Samples
SN74AHC540PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540	Samples
SN74AHC540PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74AHC540PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540	Samples
SN74AHC540PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540	Samples
SNJ54AHC540FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9685001Q2A SNJ54AHC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										540FK	
SNJ54AHC540J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685001QR A SNJ54AHC540J	Samples
SNJ54AHC540W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685001QS A SNJ54AHC540W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHC540, SN74AHC540 :

- Catalog: [SN74AHC540](#)
- Military: [SN54AHC540](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC540DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC540DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC540DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC540PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC540DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AHC540DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74AHC540DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC540PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

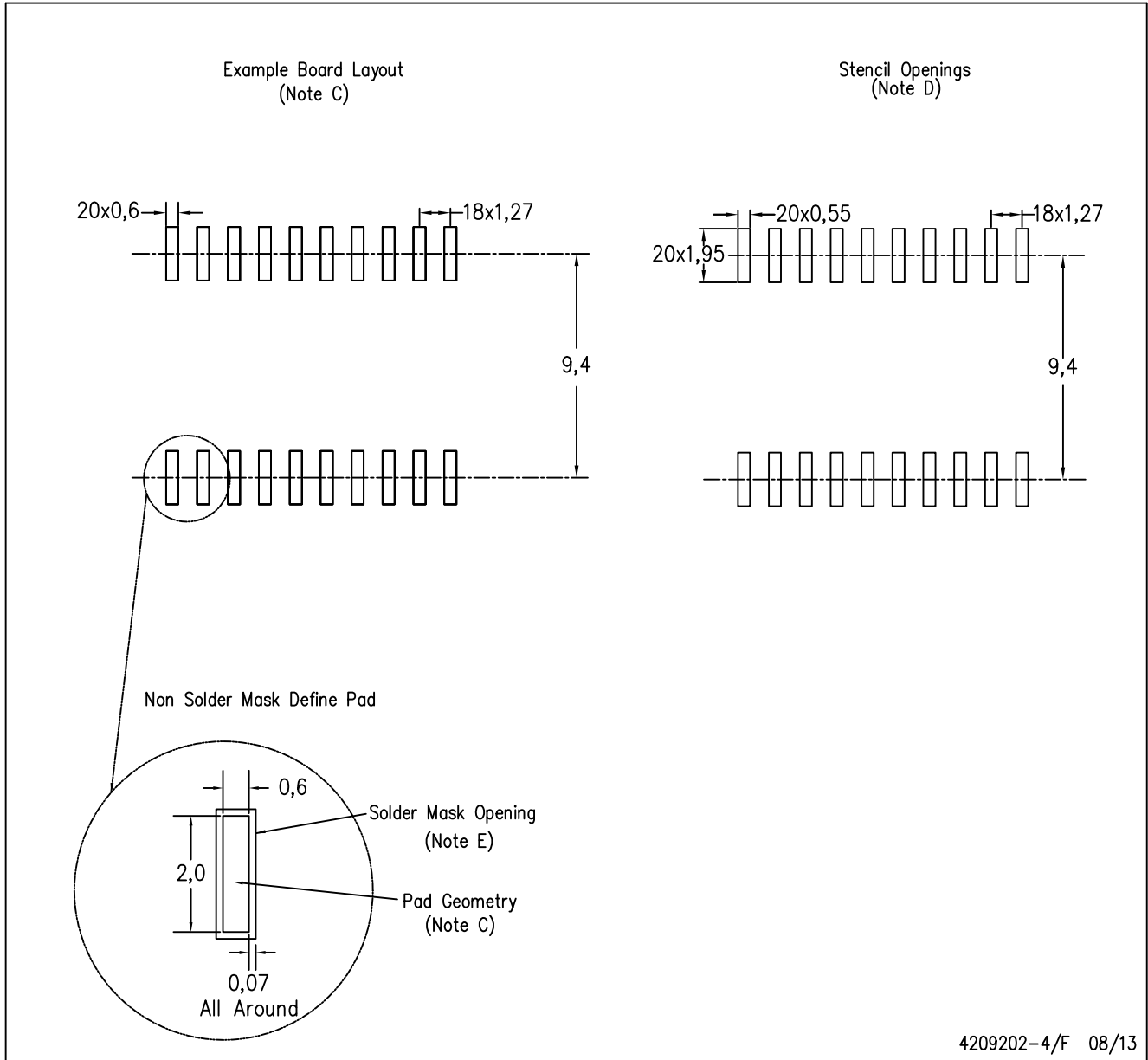
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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