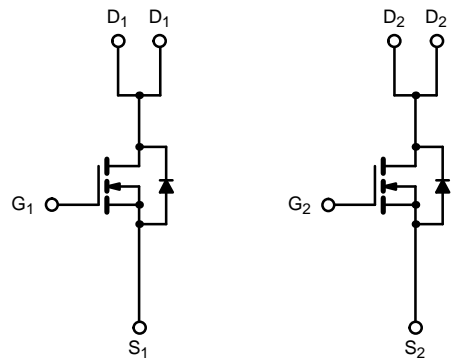
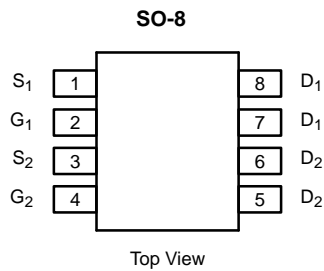




Dual N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.10 @ $V_{GS} = 10$ V	± 3.5
	0.20 @ $V_{GS} = 4.5$ V	± 2.0



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	± 14	A
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

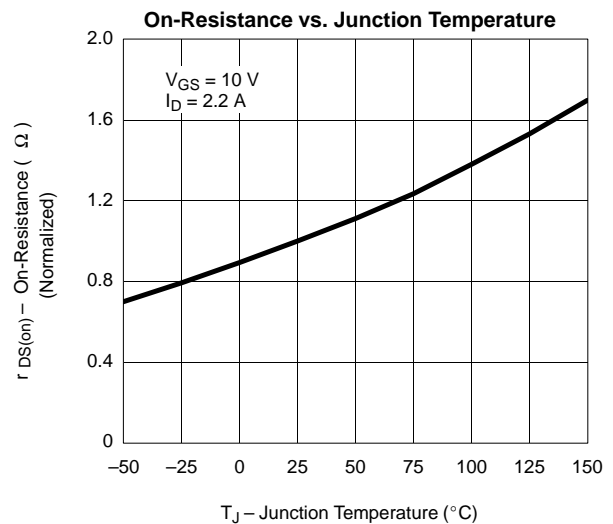
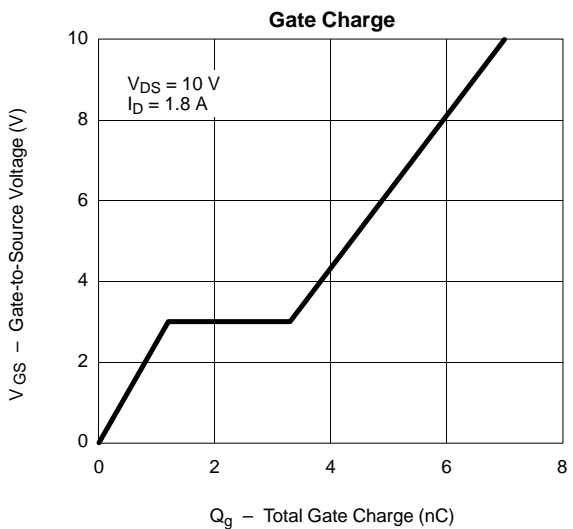
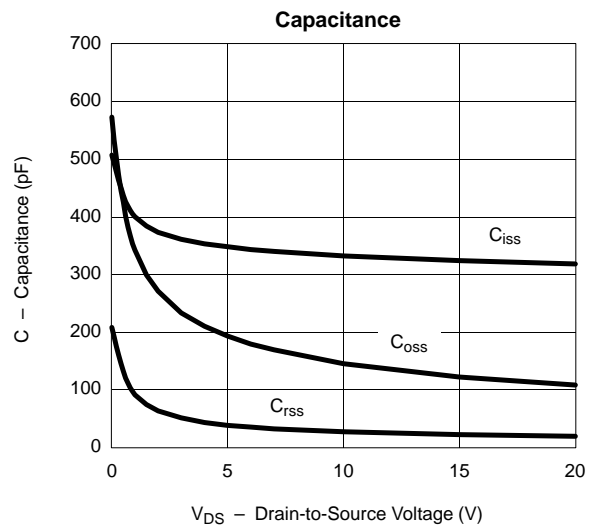
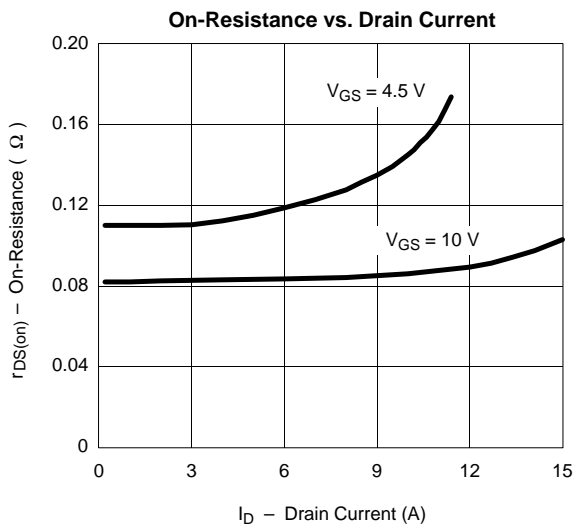
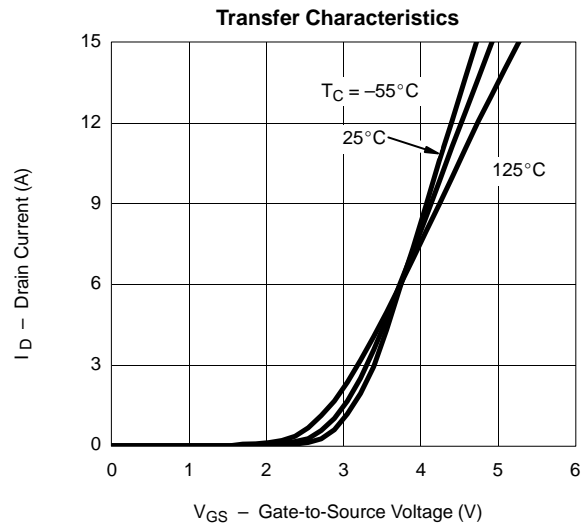
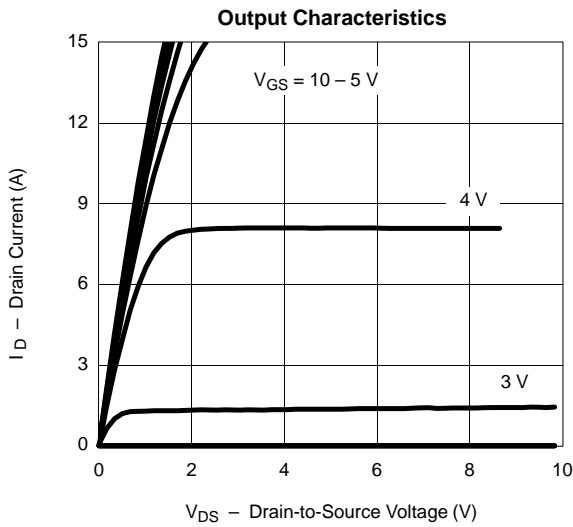


SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V			2	μA
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 55 °C			25	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	14			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 2.2 A		0.082	0.10	Ω
		V _{GS} = 4.5 V, I _D = 1 A		0.12	0.20	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 3.5 A		6.5		S
Diode Forward Voltage ^b	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V		0.75	1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 1.8 A		7	30	nC
Gate-Source Charge	Q _{gs}			1.2		
Gate-Drain Charge	Q _{gd}			2.1		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		8	20	ns
Rise Time	t _r			12	20	
Turn-Off Delay Time	t _{d(off)}			21	90	
Fall Time	t _f			8	50	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs		50	100	

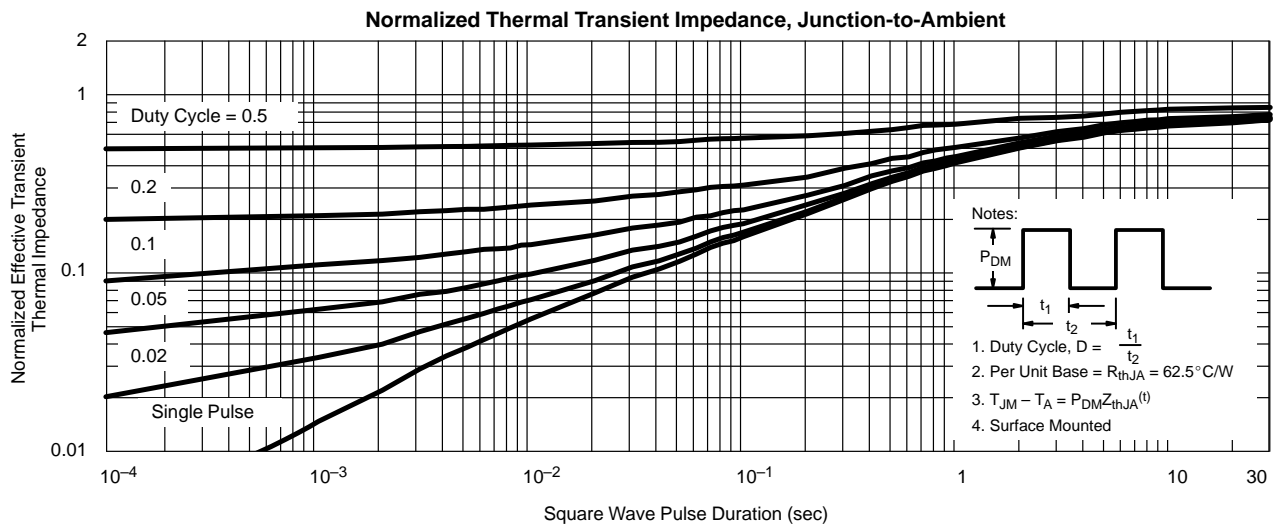
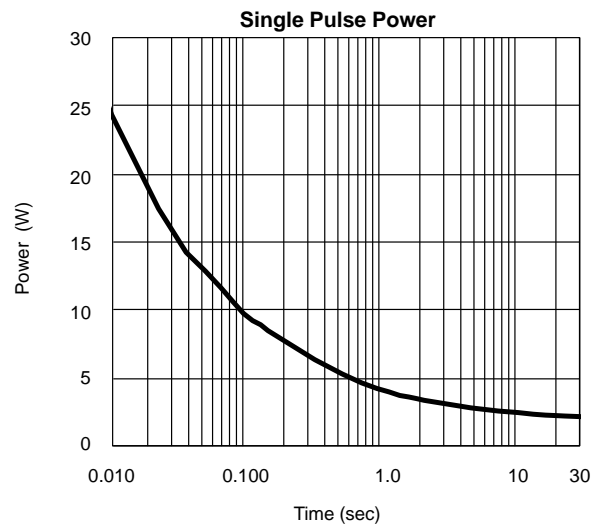
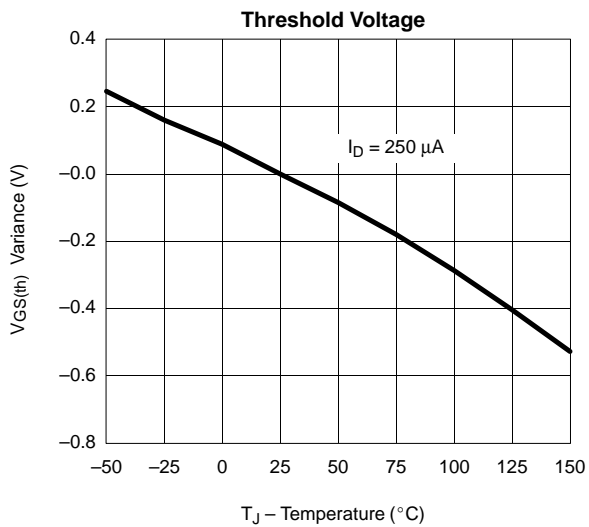
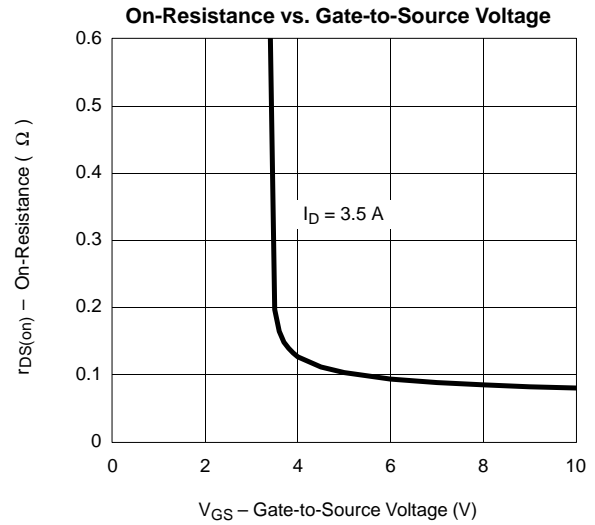
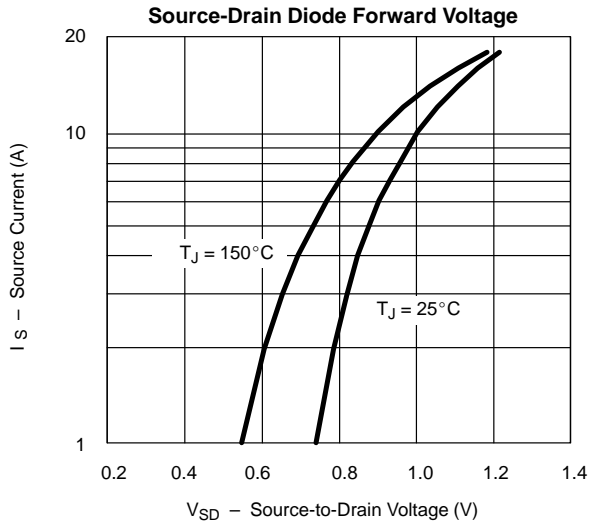
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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